CLAIMS

1. A method for verifying an integrated circuit design, comprising:

defining tasks, the tasks being formatted as text files;

identifying a test case, the test case being defined by the tasks;

correlating each of the tasks with a compiled task formatted in a hardware description language.

executing the compiled task to simulate a behavior for the integrated circuit design to determine if a goal has been achieved;

if the goal has not been achieved, the method includes adjusting the tasks of the test case; and

repeating the executing of the test case to simulate the behavior for the integrated circuit design.

2. The method of claim 1, wherein the hardware description language is verilog.

3. The method of claim 1, further comprising:

grouping the defined tasks as macrotasks.

4. The method of claim 1, wherein the method operation of identifying a test case includes,

verifying a syntax and a format of each of the tasks of the test case.

5. A method for minimizing compilation time of a test case during development testing of an integrated circuit, comprising:

identifying a test case, the test case associated with tasks written as text files;

generating a file associated with the test case;

determining a sequence of the tasks of the file;

identifying hardware description language (HDL) tasks associated with the tasks of the file according to the sequence; and

performing a simulation of an integrated circuit with the HDL tasks.

6. The method of claim 5, wherein the HDL tasks are pre-compiled.

7. The method of claim 5, wherein the method operation of generating a file associated with the test case includes,

verifying the file associated with the test case as to a syntax and a format of each of the tasks associated with the test case.

8. The method of claim 7, wherein a script performs the verification of the file associated with the test case.

9. The method of claim 5, wherein the method operation of identifying hardware description language (HDL) tasks associated with the tasks of the file according to the sequence includes,

accessing a translation layer to correlate the tasks of the file with the HDL tasks.

10. The method of claim 6, wherein the HDL tasks are stored in a library of HDL tasks on storage media in communication with a system performing the simulation.

11. The method of claim 5, wherein the HDL is verilog.

12. A computer readable medium having program instructions for avoiding re-compilation of a test case during development testing of an integrated circuit, comprising:

program instructions for identifying a test case, the test case associated with tasks written as text files;

program instructions for generating a file associated with the test case;

program instructions for determining a sequence of the tasks of the file;

program instructions for identifying hardware description language (HDL) tasks associated with the tasks of the file according to the sequence; and

program instructions for performing a simulation of an integrated circuit with the HDL tasks.

13. The computer readable medium of claim 12, wherein the program instruction for generating a file associated with the test case includes,

program instructions for verifying the file associated with the test case as to a syntax and a format of each of the tasks associated with the test case.

14. The computer readable medium of claim 13, wherein the program instructions for verifying the file associated with the test case as to a syntax and a format of each of the tasks associated with the test case include,

executing a script capable of reading the file associated with the test case.

15. The computer readable medium of claim 12, wherein the program instructions for identifying hardware description language (HDL) tasks associated with the tasks of the file according to the sequence include,

program instructions for accessing a translation layer to correlate the tasks of the file with the HDL tasks.

16. The computer readable medium of claim 12, wherein the HDL tasks are pre-compiled.

17. A computer system for validating an integrated circuit design, comprising:

a processor;

a memory;

a storage device; the storage device configured to store compiled tasks written in a hardware description language (HDL) for testing the functional characteristics of an integrated circuit design, each of the compiled tasks associated with a corresponding text file; and

a bus enabling communication between the processor, the memory and the storage device.

18. The system of claim 17, wherein the storage device is externally located from the system.

19. The system of claim 17, wherein the corresponding text file is verified as to syntax and format.

20. The system of claim 17, wherein the HDL is verilog.